UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,772	01/14/2004	Francesco Pappalardo	854063.740	5496

38106 7590 03/24/2008

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 5400
SEATTLE, WA 98104-7092

EXAMINER	
HOUSHMAND, HOOMAN	
ART UNIT	PAPER NUMBER
2619	
MAIL DATE	DELIVERY MODE
03/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,772	PAPPALARDO ET AL.	
	Examiner	Art Unit	
	Hooman Houshmand	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendments and accompanying remarks, filed on 12/12/2007, have been entered and have been fully considered. New claims 22-24 are added. Claims 1-21 have been amended. Claims 1-24 are now pending.

2. No specific portions of the original disclosure have been pointed to as to the source of the amendments and the additional new claims.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "common clock signal" newly amended to claims 1, 8, 12, 13, 17 must be shown or the feature(s) canceled from the claim(s). The "common clock" recited in the newly added claim 22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-7, 8-12, 13-16, 17-20, 21, 22-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. "common clock signal" is recited in newly added limitation to Claims 1, 8, 12, 13, 17; however, no specific portions of the original disclosure has been pointed to, in the accompanying remarks to the amendments, that contain this new limitation. "common clock signal" was not located in the original specification, claims, or drawings. For the purposes of comparison with prior art "common clock signal" is considered equivalent to

synchronization signal. “common clock” is recited in the newly added claim 22. “common clock” was not located in the original specification, claims, or drawings. For the purposes of comparison with prior art “common clock” is considered equivalent to synchronization signal. “a register to store sorting patterns” is recited in the newly added claim 23. “a register to store sorting patterns” was not located in the original specification, claims, or drawings.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curran (US 5572736) in view of Szepesi (US 5680300).

Regarding **Claim 1**: Curran teaches *a method for transmitting data on a bus* (col 1 lines 16-18) *with minimization of the bus switching activity* (col 2 lines 6-8), *converting the datum* (bits) *to be transmitted from its own original format into a transmission format* (switching codes and code word col 2 lines 5-8, col 4 lines 51-59) *that reduces the bus switching activity* (minimize the number of bits which switch between the zero and one states col 2 lines 2-14), *converting including: swapping the position of one or more bits*

of the datum to be transmitted (a function of the data word to be transmitted col 2 lines 10-11), *swapping being performable according to a plurality of different variants* (the resulting code words represent the possible code words which could be transmitted col 2 lines 32-34), *each of which is identified by a respective sorting pattern* (a set of maximally distant mappings is derived col 2 lines 30-31, col 2 lines 59-65); *and selecting, between the various sorting patterns* (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35), *a sorting pattern that reduces the bus switching activity upon transmission on the bus* (the number of bus drivers to be switched reduced col 2 lines 36-37) *of the datum generated using selected sorting pattern* (switching code identifying the mapping code col 2 lines 60-63); *transmitting on the bus the datum in transmission format; transmitting on the bus the selected sorting pattern* (switching code identifying the mapping code col 2 lines 60-65); *receiving the datum in transmission format* (receiving circuit); *receiving the selected sorting pattern transmitted on the bus* (code word); *and converting the datum received from transmission format to original format using the selected sorting pattern received* (receiving circuit, maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65), *a succession of sorting patterns generated at a transmission end* (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34) *and a succession of sorting patterns generated at a reception end* (receiver generates new mappings col 4 lines 42-59) *are synchronized with each using a common clock signal* (synchronization signal, push-pull bus driver col 4 lines 6-21).

Curran may not explicitly teach push-pull bus driver used for *synchronization*.

Szepesi teaches *synchronization* with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 2**: Curran teaches *generating a succession of sorting patterns identifying all the possible swaps of the position of the bit or bits of the datum to be transmitted* (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34); *comparing the optimal - particular - sorting pattern to be transmitted with the sorting patterns generated* (set of maximally distant mappings derived col 2 lines 30-31); *generating and transmitting on the bus a synchronization* (push-pull bus driver col 4 lines 6-21) *signal upon detection of the identity* (minimally distant) *between the optimal - particular - sorting pattern to be transmitted and one of the sorting patterns generated* (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35).

Curran may not explicitly teach push-pull bus driver used for *synchronization*.

Szepesi teaches *synchronization* with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 3**: Curran teaches *receiving the selected sorting pattern transmitted on the bus includes generating a succession of sorting patterns* (mappings) *identical to, and synchronous* (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) *with, the generated succession of sorting patterns identifying all possible swaps of the position of the bit or bits of the datum to be transmitted* (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34) *and identifying the sorting pattern generated at the instant of reception of the synchronization* (push-pull bus driver col 4 lines 6-21) *signal transmitted on the bus* (At the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9), *the sorting pattern identified being identical to said selected sorting pattern to be transmitted* (receiving circuit maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65).

Curran may not explicitly teach push-pull bus driver used for *synchronization*.

Szepesi teaches *synchronization* with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 4**: Curran teaches *the sorting pattern selected reduces the bus switching activity* (zero and one switching) *to a minimum amount* (minimize the number of bits which switch between the zero and one states col 2 lines 6-7) *and the sorting pattern selected is the optimal* (reduced delta-I noise and power consumption) *sorting pattern* (the number of bit drivers which are required to switch between the zero and one position is reduced, thereby substantially reducing the delta-I noise and power consumption col 2 lines 55-58).

Regarding **Claim 5**: Curran teaches *generating a succession of sorting patterns* (set of maximally distant mappings is derived col 2 lines 30-31) *includes providing a finite state machine* (a model of the algorithm, IEEE definition) *having a number of internal states* (the generated code words) *equal to the number of possible swaps of the position of the bit or bits of the datum to be transmitted* (plurality of the generated code words, the one

which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55); *associating to each of the internal states of finite state machine a respective sorting pattern* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46); *and operating finite state machine at a given frequency so as to cause its internal state to evolve* (compute) *and generate said sorting patterns* (Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 6**: Curran teaches *generating a succession of sorting patterns includes generating a plurality of disjoint sets of sorting patterns* (set of maximally distant mappings is derived col 2 lines 30-31), *each set being formed by a sorting pattern identifying a respective subset of possible swaps of the position of the bit or bits of the datum to be transmitted* (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), *the sorting patterns of each set being further generated in succession and in a synchronous* (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) *way with respect to the sorting patterns of the other sets* (a plurality of mapping codes are generated col 4 lines 44-46).

Regarding **Claim 7**: Curran teaches *generating a plurality of separate sets of sorting patterns* (set of maximally distant mappings is derived col 2 lines 30-31) *includes, for each said set of sorting patterns, providing a finite state machine* (a model of the algorithm – IEEE definition) *having a number of internal states* (the generated code words) *equal to the number of sorting patterns in the set* (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55); *associating to each of the internal states of said finite state machine a respective sorting pattern* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46); *and operating said finite state machine at a given frequency so as to cause its internal state to evolve* (compute) *and generate the corresponding sorting patterns* (each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 8**: Curran teaches *a device and system for transmitting data on a bus* (col 1 lines 16-18) *with minimization of the bus switching activity* (col 2 lines 6-8), *first converting means for converting the datum* (bits) *to be transmitted from its own original format to a transmission format* (switching codes and code word col 2 lines 5-8, col 4 lines 51-59) *that minimizes the bus switching activity* (minimize the number of bits which switch between the zero and one states col 2 lines 2-14), *first converter means includes*

a swap operator for swapping the position of one or more bits of the datum to be transmitted (a function of the data word to be transmitted col 2 lines 10-11), *swapping being performable according to different variants* (the resulting code words represent the possible code words which could be transmitted col 2 lines 32-34), *each of which is identified by a respective sorting pattern* (a set of maximally distant mappings is derived col 2 lines 30-31); *and selecting means for selecting, between the various sorting patterns* (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35), *an optimal sorting pattern that minimizes the bus switching activity* (the number of bus drivers to be switched reduced col 2 lines 36-37) *upon transmission on the bus of the datum generated using optimal sorting pattern* (switching code identifying the mapping code col 2 lines 60-63); *transmitting means for transmitting on the bus the datum in transmission format and the optimal sorting pattern; receiving means for receiving the datum in transmission format and optimal sorting pattern* (code word) *transmitted on the bus; and second converting means for converting the datum received from transmission format to original format using optimal sorting pattern received* (receiving circuit, maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65), *transmitting means includes first sorting pattern generating means for generating a succession of sorting patterns identifying all the possible swaps of the position of the bit or bits of the datum to be transmitted* (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34); *comparing means for comparing the optimal sorting pattern to be transmitted with the sorting patterns generated* (set of maximally distant

mappings derived col 2 lines 30-31); *signal generating means for generating and sending onto bus a synchronization* (push-pull bus driver col 4 lines 6-21) *signal upon detection of the identity* (minimally distant) *between the optimal sorting pattern to be transmitted and one of the sorting patterns generated* (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35), *receiving means includes second sorting pattern generating means for generating a succession of sorting patterns* (mappings) *identical to, and synchronous* (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) *with, the sorting patterns generated by the first sorting pattern generating means for transmission* (receiver applies reverse mapping to recover the original data word, it makes a state transition form the last state it was in to a new state, col 4 lines 57-59); *and detecting means for identifying the sorting pattern generated by second sorting pattern generating means at the instant of reception of the synchronization* (push-pull bus driver col 4 lines 6-21) *signal transmitted on the bus* (at the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9), *the sorting pattern identified being identical to optimal sorting pattern to be transmitted* (receiving circuit maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65), *a succession of sorting patterns generated at a transmission end* (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34) *and a succession of sorting patterns generated at a reception end* (receiver generates new mappings col 4

lines 42-59) are synchronized with each using a common clock signal (synchronization signal, push-pull bus driver col 4 lines 6-21).

Curran may not explicitly teach: push-pull bus driver used for *synchronization*.

Szepesi teaches: *synchronization* with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field, their art is analogous.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 9**: Curran teaches *first and second sorting pattern generating means each comprise a finite state machine* (a model of the algorithm – IEEE definition) *having a number of internal states* (the generated code words) *equal to the number of possible swaps of the position of the bit or bits of the datum to be transmitted* (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), *a respective sorting pattern* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46) *being associated to each of the internal states of finite state machine, finite state machine being operated at a given frequency so as to cause its internal state to evolve* (compute) *and generate sorting patterns* (each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word

are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 10**: Curran teaches *first and second sorting pattern generating means each comprise a plurality of sorting pattern modules generating a plurality of disjoint sets of sorting patterns* (set of maximally distant mappings is derived col 2 lines 30-31), *each set being formed by a sorting pattern identifying a respective subset of all the possible swaps of the position of the bit or bits of the datum to be transmitted* (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), *the sorting patterns of each set being further generated in succession and in a synchronous* (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) *way with respect to the sorting patterns of the other sets* (a plurality of mapping codes are generated col 4 lines 44-46).

Regarding **Claim 11**: Curran teaches *each sorting pattern* (set of maximally distant mappings is derived col 2 lines 30-31) *generating modules comprises a finite state machine* (a model of the algorithm – IEEE definition) *having a number of internal states* (the generated code words) *equal to the number of sorting patterns of the corresponding set* (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), *a respective sorting pattern being associated to each of the internal states of*

said finite state machine (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46), *finite state machine being operated at a given frequency so as to cause its internal state to evolve* (compute) *and generate sorting patterns* (each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 12**: Curran teaches *a computer product* (col 1 line 16) *loadable into a memory associated with a bus, said computer product having portions of software code that* (computer system, data is transmitted as a multi-bit data word between units such as processors and memories, by means of bus driver circuits col 1 lines 16-18) *are executable by a processor to minimize bus switching activity* (minimize the number of bits which switch between the zero and one states col 2 lines 2-14), *by converting a datum to be transmitted from its own original format into a transmission format that reduces the bus switching activity* (a function of the data word to be transmitted col 2 lines 10-11), *converting includes swapping a position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants* (The resulting code words represent the possible code words which could be transmitted col 2 lines 32-34), *each of which is identified by a respective sorting pattern* (a set of maximally distant mappings is derived col 2 lines 30-31); *and selecting, between the sorting patterns* (the code word which is minimally distant from the

previous code word is selected col 2 lines 34-35), *a particular sorting pattern that reduces the bus switching activity* (the number of bus drivers to be switched reduced col 2 lines 36-37) *upon transmission on the bus of the datum generated using selected sorting pattern* (switching code identifying the mapping code col 2 lines 60-63); *transmitting on the bus the datum in said transmission format; and transmitting on the bus a synchronization* (push-pull bus driver col 4 lines 6-21) *signal usable by a receiving device to identify selected sorting pattern from sorting patterns* (at the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9), *a succession of sorting patterns generated at a transmission end* (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34) *and a succession of sorting patterns generated at a reception end* (receiver generates new mappings col 4 lines 42-59) *are synchronized with each using a common clock signal* (synchronization signal, push-pull bus driver col 4 lines 6-21).

Curran may not explicitly teach: push-pull bus driver used for *synchronization*.

Szepesi teaches: *synchronization* with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 13**: Curran teaches *transmitting n-bit data on a single line, generating in succession all the possible combinations of n bits* (code words col 2 lines 31-35); *comparing the n-bit datum to be transmitted with the combinations of n bits generated* (set of maximally distant mappings derived col 2 lines 30-31); *generating and transmitting on a single line an identity signal* (minimally distant) upon *detection of the coincidence between the n-bit datum to be transmitted and one of the combinations of n bits generated* (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35) , *and in reception, generating a succession of combinations of n bits* (mappings) *identical and synchronous to the combinations generated in succession in transmission* (receiver applies reverse mapping to recover the original data word col 4 lines 57-59, the receiver transitions from the previous state to the new state, mapping codes are generated col 4 lines 42-59); *and identifying the combination of n bits generated at the instant of reception of the identity signal transmitted on the single line* (at the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9), *the combination of n bits identified being identical - corresponding - to the n-bit datum to be transmitted* (receiving circuit maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65), *a succession of*

sorting patterns generated at a transmission end (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34) *and a succession of sorting patterns generated at a reception end* (receiver generates new mappings col 4 lines 42-59) *are synchronized with each using a common clock signal* (synchronization signal, push-pull bus driver col 4 lines 6-21).

Curran may not explicitly teach: push-pull bus driver used for *synchronization*.

Szepesi teaches: *synchronization* with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 14**: Curran teaches *generating in succession all the possible combinations of n bits* (set of maximally distant mappings is derived col 2 lines 30-31), *in transmission and reception* (corresponding states exit at both the transmitter and receiver - the code words. The switch bits indicate which state to transition to next. These switch bits are calculated at the transmitter, and communicated to the receiver 4:42-59), *includes providing a finite state machine* (a model of the algorithm – IEEE definition) *having a number of internal states* (the generated code words) *equal to the*

number of possible combinations of n bits (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55); *associating to each of the internal states of finite state machine a respective combination of n bits* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46); *and operating finite state machine at a given frequency so as to cause its internal state to evolve (*compute*) and generate the corresponding combinations of n bits* (each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 15**:

Curran teaches *generating the combinations of n bits includes generating a plurality of disjoint sets of possible combinations of n bits* (set of maximally distant mappings is derived col 2 lines 30-32), *in transmission and reception* (corresponding states exit at both the transmitter and receiver - the code words. The switch bits indicate which state to transition to next. These switch bits are calculated at the transmitter, and communicated to the receiver 4:42-59), *the combinations of n bits of each set being further generated in succession and in a synchronous* (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) way with

respect to the combinations of n bits of the other sets (a plurality of mapping codes are generated col 4 lines 44-46).

Regarding **Claim 16**: Curran teaches, *in transmission and reception* (corresponding states exit at both the transmitter and receiver, the code words. The switch bits indicate which state to transition to next. These switch bits are calculated at the transmitter, according to the data to be transmitted, and communicated to the receiver 4:42-59), *generating a plurality of disjoint sets of possible combinations of n bits* (set of maximally distant mappings is derived col 2 lines 30-32) *includes, for each set of combinations of n bits, providing a finite state machine* (a model of the algorithm – IEEE definition) *having a number of internal states* (the generated code words) *equal to the number of combinations of n bits in the set* (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55); *associating to each of the internal states of finite state machine a respective combination of n bits* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46); *and operating finite state machine at a given frequency so as to cause its internal state to evolve* (compute) *and generate the corresponding combinations of n bits* (each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 17**: Curran teaches *a system for transmitting n-bit data on a single line, including, at the transmission end: first combination generating means for generating in succession all the possible combinations of n bits* (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34); *comparing means for comparing the n-bit datum to be transmitted with the combinations of n bits generated* (set of maximally distant mappings derived col 2 lines 30-32); *signal generating means for generating and transmitting on a single line an identity signal upon detection* (minimally distant) *of the coincidence between the n-bit datum to be transmitted and one of the combinations of n bits generated* (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35); *at the reception end: second combination generating means for generating the same succession of combinations of n bits* (receiver applies reverse mapping to recover the original data word col 4 lines 57-59, the state transitions to the new state), *generated by the first combination generating means, the successions of combinations of n bits as that generated by the said first and second combination-generating means being synchronized* (push-pull bus driver col 4 lines 6-21; instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) *with one another; and detecting means for identifying the combination of n bits generated, by receiver, at the instant of reception of the identity signal transmitted on the single line* (at the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9) , *the combination of n bits*

identified being identical, corresponding, to the n-bit datum to be transmitted (receiving circuit maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65), *a succession of sorting patterns generated at a transmission end* (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34) *and a succession of sorting patterns generated at a reception end* (receiver generates new mappings col 4 lines 42-59) *are synchronized with each using a common clock signal* (synchronization signal, push-pull bus driver col 4 lines 6-21).

Curran may not explicitly teach: push-pull bus driver used for *synchronization*.

Szepesi teaches: *synchronization* with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 18**: Curran teaches *a finite state machine* (a model of the algorithm – IEEE definition) *having a number of internal states* (the generated code words) *equal to the number of possible combinations of n bits* (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously

transmitted code word is selected col 2 lines 51-55), *a respective combination of n bits being associated to each of the internal states of finite state machine* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46) , *and finite state machine being operated at a given frequency so as to cause its internal state to evolve* (compute) *and generate the corresponding combinations of n bits* (each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 19**: Curran teaches *combination generating modules generating a plurality of disjoint sets of possible combinations of n bits* (set of maximally distant mappings is derived col 2 lines 30-32), *the combinations of n bits of each set being generated in succession and in a synchronous* (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-44) way with respect to the combinations of n bits of the other sets (a plurality of mapping codes are generated col 4 lines 44-46).

Regarding **Claim 20**: Curran teaches *combination generating modules* (set of maximally distant mappings is derived col 2 lines 30-31) *comprises a finite state machine* (a model of the algorithm – IEEE definition) *having a number of internal states* (the generated code words) *equal to the number of combinations of n bits in the set* (plurality of the

generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), *a respective combination of n bits being associated to each of the internal states of finite state machine* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46) , *and finite state machine being operated at a given frequency so as to cause its internal state to evolve* (compute) *and generate the corresponding combinations of n bits* (each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 21**: Curran teaches *a computer product* (col 1 line 16) *loadable into memory, including software code that implement the method* (computer system, data is transmitted as a multi-bit data word between units such as processors and memories, by means of bus driver circuits col 1 lines 16-18) *when the computer product is executed by a digital processor associated to the bus* (col 1 lines 17-18).

Regarding **Claim 22**: Curran teaches *a transmitter device* (col 1 lines 16-18), *a converter to convert a datum to be transmitted from an initial format to a transmission format* (switching codes and code word col 2 lines 5-8, col 4 lines 51-59), *transmission format being a selected sorting pattern from among a succession of sorting patterns that*

identify possible swaps of bit positions of datum (the resulting code words represent the possible code words which could be transmitted col 2 lines 32-34); *a first finite state machine having a number of internal states* (the generated code words) *equal to a number of sorting patterns* (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55) *and each of internal states respectively corresponding to one of sorting patterns* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46); *and a common clock* (synchronization signal, push-pull bus driver col 4 lines 6-21) *adapted coupled to first finite state machine* (IEEE definition: a computational model consisting of a finite number of states and transitions between those states, possibly with accompanying actions) *to synchronize first finite state machine with a second finite state machine, at a receiving end* (corresponding states exit at both the transmitter and receiver - the code words. The switch bits indicate which state to transition to next. These switch bits are calculated at the transmitter, and communicated to the receiver 4:42-59), *that receives datum in transmission format* (switching codes and code word col 2 lines 5-8, col 4 lines 51-59) *and that has a number of internal states* (the generated code words) *equal to number of sorting patterns* (resulting code words represent the possible code words col 2 lines 32-34) *and each of internal states of second finite state machine at the receiving end respectively corresponding to one of sorting patterns, first finite state machine is adapted to generate a synchronization signal to be received by second state machine, synchronization signal* (push-pull bus driver col 4 lines 6-21) *corresponding to a particular state of first finite*

state machine and adapted to be used by second finite state machine to identify selected sorting pattern (switching code identifying the mapping code col 2 lines 60-63) (the generated code word which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55).

Curran may not explicitly teach: push-pull bus driver used for *synchronization*.

Szepesi teaches: *synchronization* with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 23**: Curran teaches (7:16-47) *a register to store sorting patterns*.

Regarding **Claim 24**: Curran teaches *sorting patterns are from among a plurality of disjoint sets of sorting patterns* (set of maximally distant mappings is derived col 2 lines 30-31).

Response to Arguments

6. Applicant's arguments filed 12/12/2007 have been fully considered but they are not persuasive.

7. The main argument on pages 12-13 is that the limitation of a *finite state machine* has not been met. Examiner respectfully disagrees. A *finite state machine* is well known in the art. The standard definition from "The authoritative dictionary of IEEE standard terms, seventh edition" is: "finite state machine (software) *A computational model consisting of a finite number of states and transitions between those states, possibly with accompanying actions*". "a model of the algorithm" pointed to in the office action is from this definition. A discussion of how the limitation of a *finite state machine* has been met follows: *a) finite number of states*: (the code words col 4 lines 42-59) *b) a computational model* (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46) (each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57) *c) transitions between those states*: (The code word with the lowest Hamming distance is transitioned to col 4 lines 51-57) *d) accompanying actions*: (receiver recovers the original data word col 4 lines 42-59)

8. A second argument on pages 12-13 is that the *FSM is located at both the transmitter and receiver*, the reference teaches this limitation (corresponding states exit at both the transmitter and receiver - the code words. The switch bits indicate which

state to transition to next. These switch bits are calculated at the transmitter, and communicated to the receiver 4:42-59).

9. The third argument on pages 13-15 is regarding *synchronization*. The references teach this limitation: A push-pull bus driver (col 4 lines 6-21) has been pointed to at the office action. A further discussion to clarify the teachings of the reference follows: (col 4 lines 6-21): {transmitted via set of bus drivers 111 which transmit the code words on external bus 121 (Fig. 1 shows a drawing of these elements). The bus drivers 111 are CMOS bus drivers (push-pull driver) which are well known in the art.} It is well known in the art that transmitters and receivers synchronize using the activity on the bus that connects them. When the transmitter is transmitting on the Bus 121, using the push-pull drivers, given the time delay of the propagation to the receiver, the receiver senses the activity on the bus line and recovers timing from the changes in voltage levels. The primary reference by itself can be relied upon to teach *synchronization* using the knowledge of a person of ordinary skill in the art. To make the teachings of *synchronization* explicit, a secondary reference, Szepesi, was brought in that shows the details of the circuits for driving lines and explicitly states that it is used for *synchronization* (col 6 lines 18-34 *synchronization* block 22).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hooman Houshmand whose telephone number is (571)270-1817. The examiner can normally be reached on Monday - Friday 8 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hooman Houshmand/
Examiner, Art Unit 2619
March 10, 2008

/Hassan Kizou/
Supervisory Patent Examiner, Art Unit 2619